**What did you do?**

We verify the VIH ,VIL ,VOH and VOL for gate(TTL&CMOS) and differ between them

**How did you do it?**

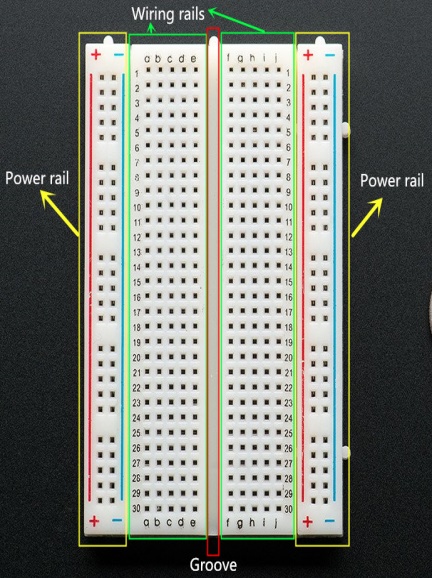
We connect IC(74SL04, 74HC04) to breadboard and connect IC by pin 14 to + and by pin 7 with - .

We connect wire with pin(1) and use it as input pin . the pin 2 is output pin . after that we measure vout at pin 2 .finally we built table for value of Vout.

**What did you find?**

We find VIH ,VIL ,VOH and VOL for TTL and CMOS gates.(you find the result below)

**Introduction:**

In this experiment , we will Know what is the practical difference (in terms of voltages) between logic 0 and logic 1, understand the significance of VOH,VOL,VIH and VIL , determine the noise margins for TTL and CMOS inverter, understand the differences between logic levels for CMOS and TTL gates and obtain the voltage transfer characteristic (VTC) for TTL and CMOS inverters.

**Tools:**

1. **Breadboard**
2. **Wires**
3. **Digital Multimeter**
4. **Power supply**
5. **ICs & Datasheet:**
6. **7408 (AND Gate)**
7. **7432 (OR Gate)**
8. **7400 (NAND Gate)**
9. **7404 (INVERT Gate)**

**Procedure:**

1. we turn the power supply and check if it work in right way and check the wires

with multimeter.

2. We use channel 3 (fixed five voltage) and set the voltage at 5V .

3. We connect the + terminal from the ch3 in power supply with red power rail ‘+’ line in breadboard and the – terminal with the blue power rail ‘-‘ line in breadboard.

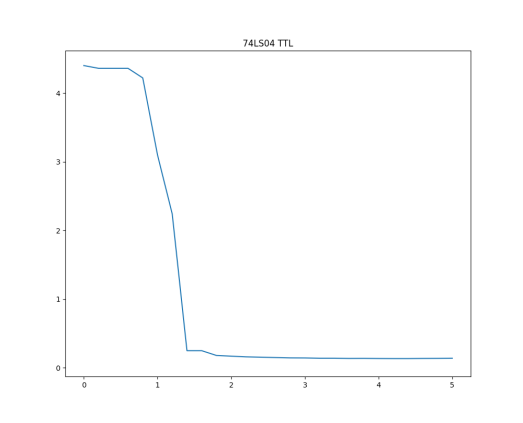
4. For ICs ,for each one we connect 14-pin (VCC)with red power rail ’+’ line and 7-pin (GND) with blue power rail’-‘ line.

5 . we use ch2 to give different voltage (0-5) we connect GND with with blue power rail’-‘ line and connect + wire with pin 1 in ICS.

1. Connect pin 2 with multimeter to measure vout.
2. Input different voltage and record it .
3. Repeat the previous step to second gate.

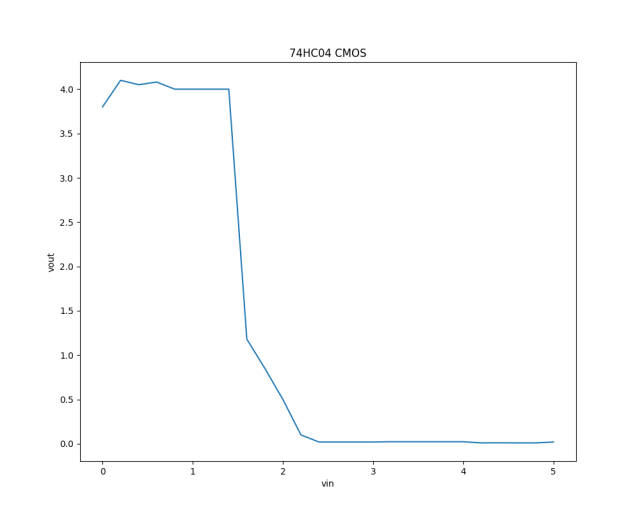
**Result:**

**a-74LS04: b-74HC04**

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|  |  |
| --- | --- |
| X values | Y values |
| 0 | 3.8 |
| 0.2 | 4.1 |
| 0.4 | 4.05 |
| 0.6 | 4.08 |
| 0.8 | 4 |
| 1 | 4 |
| 1.2 | 4 |
| 1.4 | 4 |
| 1.6 | 1.18 |
| 1.8 | 0.85 |
| 2 | 0.5 |
| 2.2 | 0.1 |
| 2.4 | 0.02 |
| 2.6 | 0.02 |
| 2.8 | 0.02 |
| 3 | 0.02 |
| 3.2 | 0.023 |
| 3.4 | 0.023 |
| 3.6 | 0.023 |
| 3.8 | 0.023 |
| 4 | 0.023 |
| 4.2 | 0.01 |
| 4.4 | 0.011 |
| 4.6 | 0.01 |
| 4.8 | 0.01 |
| 5 | 0.02 |

|  |  |
| --- | --- |
| X values | Y values |
| 0 | 4.4 |
| 0.2 | 4.36 |
| 0.4 | 4.36 |
| 0.6 | 4.36 |
| 0.8 | 4.22 |
| 1 | 3.1 |
| 1.2 | 2.24 |
| 1.4 | 0.25 |
| 1.6 | 0.25 |
| 1.8 | 0.18 |
| 2 | 0.17 |
| 2.2 | 0.16 |
| 2.4 | 0.155 |
| 2.6 | 0.15 |
| 2.8 | 0.145 |
| 3 | 0.144 |
| 3.2 | 0.14 |
| 3.4 | 0.14 |
| 3.6 | 0.137 |
| 3.8 | 0.138 |
| 4 | 0.136 |
| 4.2 | 0.135 |
| 4.4 | 0.135 |
| 4.6 | 0.137 |
| 4.8 | 0.138 |
| 5 | 0.14 |

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **From graph** | **From**  **datasheet** |  |  | **From graph** | **From**  **datasheet** |
| **VIL** | **0.8** | **0.8** |  | **VIL** | **1.4** | **1.4** |
| **VIH** | **1.7** | **2** |  | **VIH** | **2.4** | **3.15** |
| **VOL** | **0.2** | **0.5** |  | **VOL** | **0.02** | **0.1** |
| **VOH** | **4.2** | **2.7** |  | **VOH** | **4** | **4.4** |

Noise Margin Low ( NML ) = VIL – VOL =0.8 – 0.2 = 0.6

Noise Margin High ( NMH)  = VOH – VIH  = 4.2 – 1.7= 2.5

Noise Margin Low ( NML ) = VIL – VOL =1.4 – 0.02 = 1.38

Noise Margin High ( NMH)  = VOH – VIH  = 4 – 2.4= 2.6

**Discussion :**

When we compare practical value with data sheet .we found practical result is accepted result , but we have error because human error , error through The production process or error in devices and items: ( multmeter , IC , breadboard).

**Conclusion :**

After doing this experience we know how to distinguish between logic 1 and logic 0 and what this meaning in term of voltages , “ acceptable “ input signal voltages range and “ acceptable “ output signal voltages range .

We also calculate the noise margin which mean the difference between the acceptable output and input ranges .

CMOS gate circuits have input and output signal specifications that are quite different from TTL .